6.012 Final Project

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September 27, 2022

1 Design Requirements

For this project, SAMTEL selected an ARM Processor, and requests a microprocessor design that consumes the minimum amount of energy given the follow constraints.

- Operating Speed 200 MHz
- V_{dd} must be between 400 mV and 4 V
- No features < 4 nm
- Height of the metal gate, source, and drain electrodes are fixed
- Total length of entire transistor is fixed at 175 nm
- Maximum doping values cannot exceed $1E20$ /cm3

2 Final Optimized Transistor Design

Using simulations in Sentaurus, we were able to optimize the design of the given ARM processor to simulate its performance given changes to its physical constraints. Throughout the course of the design project, we experimented with the impact of changes in physical dimensions (oxide thickness, doping concentration), as well as material changes in an effort to minimize the power loss of our transistor. The key modifications we made to the existing transistor, and its general composition are outlined in the diagram below.

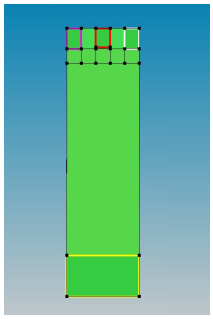

Figure 1: General Structure of Final Transistor Design

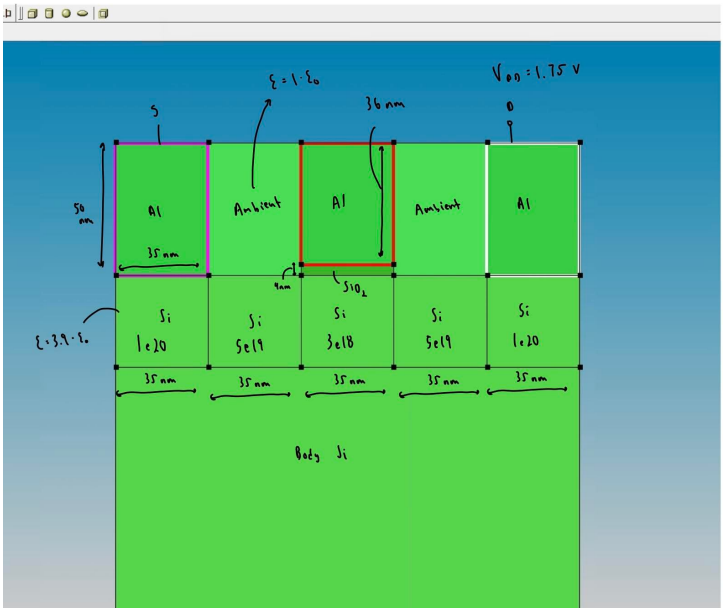

Figure 2: Close up Breakdown

3 Summary of Key Changes Made

With the 200 MHz clock speed and minimum energy expenditure as our primary constraints, we propose the following changes to the existing ARM Processor.

1. Decreasing oxide thickness, t_{oxide}, to 4 nms.
2. Changing the material composition of the left and right spacers from SiO_2 to Ambient.
3. Increasing the doping concentrations of the Source and Drain to the upper limit of $1e20/cm^{-1}$
4. Lowering the supply voltage to $V_{dd} = 1.75V$

4 Performance of Optimized Transistor

Our final proposed transistor design operates at a V_{dd} of 1.75 V and has an I_{on} of 740.727 $\frac{\mu A}{\mu m}$. It has an off current I_{off} of 402.766 $\frac{nA}{\mu m}$ as well as a clock frequency, of 208 Mhz. Most notably, we were able to reduce the EDP to 182.5 $ns * pJ$ while decreasing Leakage Energy (27.82 pJ), Dynamic Energy(10.2 pJ), and Total Energy Expenditure(38.02 pJ).

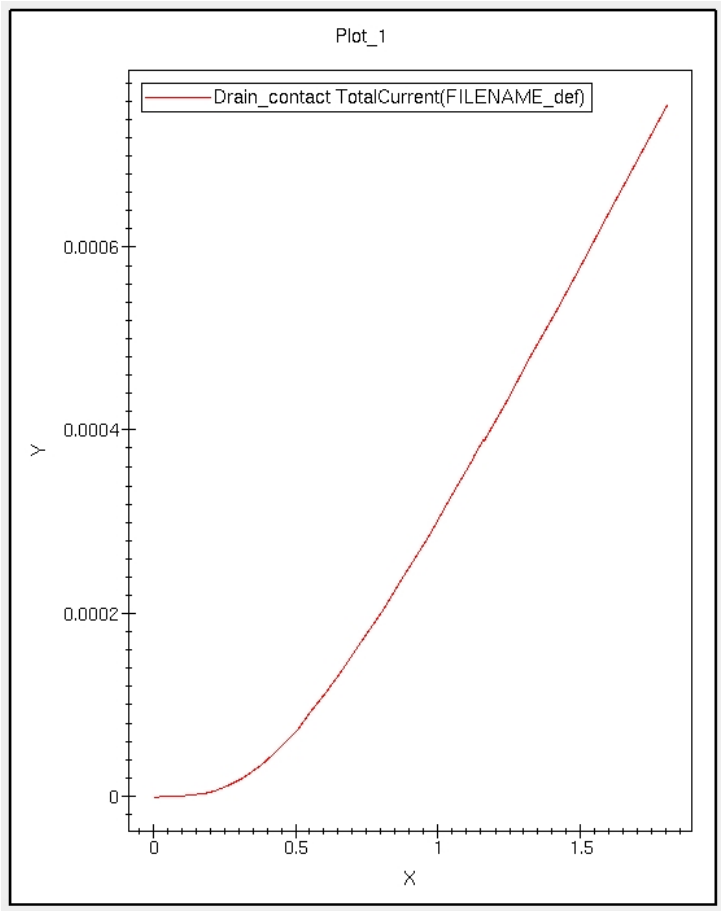

Figure 3: IV Characteristic Plot Final Transistor Design

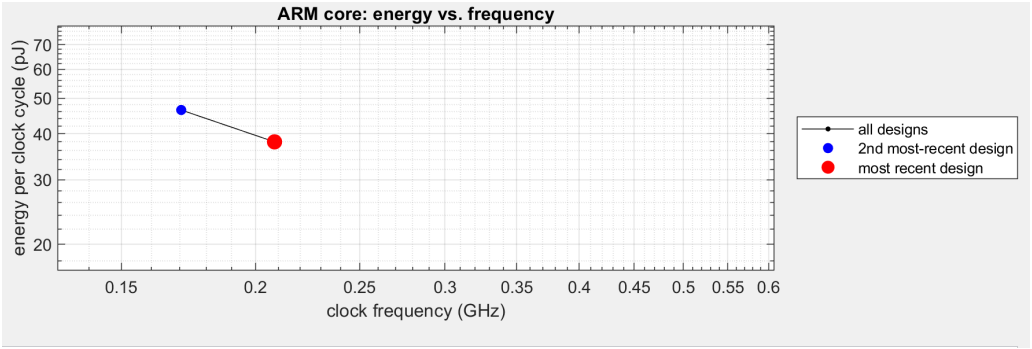

Figure 4: ARM Core energy vs frequency, Final Transistor Design (Red), Original (Blue)

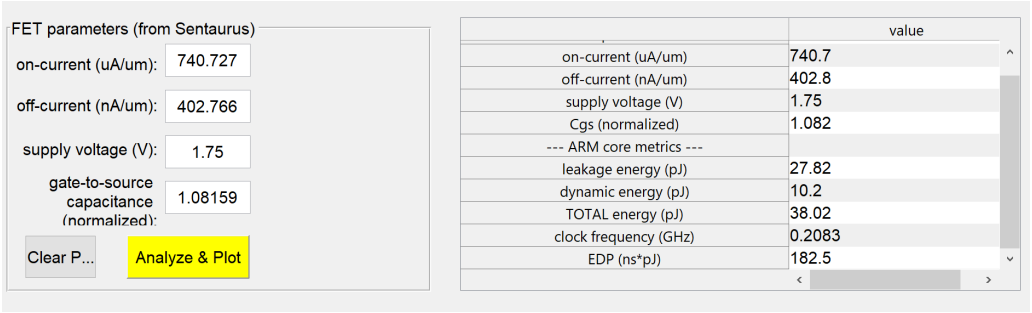

Figure 5: Final MOSFET Design Parameters, EDP, and Clock Frequency

5 General Approach

Our general approach to finding an optimal transistor layout, was first to run the original transistor and see how far off the key values were most notably EDP and Clock frequency. After taking note of the existing parameters, we noted that given what we had learned in lecture and over the course of the semester, changing one parameter at a time, assessing its result and then combining all of them at the end was not a functional solution. Even more so when one considers the interdependence that each of the physical constraints have on one another. As a result, German and I decided to build our transistor design sequentially, essentially, we would make a design choice that would get us closer to our goal, assess what problems had arisen from the change, and make an informed decision on our next modification to move us in the right direction. Using this method, we were able to meet spec.

To begin, we first decided to look at the equations for EDP, and clock frequency, in order to see what knobs we could turn and what expected outcomes we should see given those changes.

$$t_{clk} = LD*(1/2)*log(2)*(R_{on}*(C_{out}+C_{wire}*l_{wire}+FO*C_{in})+(R_{wire}*l_{wire})*((C_{wire}*l_{wire}*0.5)+FO*C_{in}))$$

$$EDP = LG*S*(((V_{dd}^2)/R_{off})*t_{CLK}+a*((C_{out}+(C_{wire}*l_{wire})+FO*C_{in})*V_{dd}^2))*t_{CLK}$$

Using this, the primary "knobs" that we see are the capacitances, as a result, the first portion of our approach focused on reducing the parasitic capacitances that exist in our MOSFET. In doing so, we could minimize the energy lost in the dielectric and the spacers.

$$C = \frac{A * e_0}{t_{oxide}}$$

For our first change, we decided to reduce the oxide thickness, while this seems counter intuitive, we were first concerned with achieving clock frequency spec. By reducing our

oxide thickness, our MOSFET is more receptive to our gate voltage, allowing it to switch more quickly. We can thereby improve our clock frequency, but at the cost of increasing our capacitance. We wanted to see how far behind we were starting before going ahead and fixing the associated problems. Essentially, the thinner oxide (4 nm) causes us to incur leakage effects etc. but we figured that we could rectify this after the fact. We reduced this to the minimum and were presented with an increase in total energy as we expected. However, our EDP actually decreased to 249.3 since our clock frequency increased to 193 MHz.

For our next change, we drastically needed to reduce our capacitances elsewhere, in order to make up for our change in the oxide. In our calculations of leakage capacitance, we realized that the component of the capacitance that resulted from the spacer was much larger than that of the oxide. As a result, we decided to switch out the material here to one with a smaller permittivity. As in the equation above, decreasing $epsilon_0$ should decrease our capacitance. Here, we opted for the lowest option we had, Ambient, with a permittivity of $1 * 8.854 * 10^-12$. The impact that this had was surprising. To have hit spec after only two changes was particularly noteworthy. Changing the spacer material brought out leakage capacitance ratio closer to 1, (1.082), and this had drastic effects on our EDP and Clock Frequency. Our EDP decreased further to 217.1 and our clock frequency increased to 208 MHz, both well within spec. Using SiO2 in the spacers seemed to provide only negative effects, something we noted.

After making the change to the spacers, our next train of thought led us to optimizing the doping in the drain and source. Changing the doping in the source and drain would hopefully allow us to increase I, as well as increase the number of charge carriers in the channel. We maxed this quantity out to $1e20$, but since the current design was already very close to the maximum these results were negligible.

After this last change, we had met spec. However, out of curiosity, we experimented with doubling the channel doping, and modifying the material composition of the oxide. Changing the oxide material to HfO2 and GaAs only led us to negative effects which made sense. These were selected based on research and availability in the Sentaurus. Hf02 has a permittivity of 16, which only increased our capacitances. As we discussed in class, the need for new materials was predicated on avoiding short channel effects, and leakage currents. If we increase the permittivity without properly adjusting the area, we would only increase our losses. As a result, we decided against this change and kept our current design. Doubling the doping in the channel killed our mobility and in turn our current. This destroyed our clock frequency as expected so we avoided this change as well.

	A	B	C	D	E	F	G
1		Sentaurus Ouputs					
2		N/A	M1	M2	M3	M4	M5
3		Standard	Oxide Thickness (5nm->4nm	Spacers (Ambient)	Maximum Doping (1 e20)	Double Channel Doping (6 e18)	Changing oxide material (Hf02)
4	V_dd (V)	1.8	1.8	1.8	1.8	1.8	1.8
5	I_on (A/um)	0.000587941	0.000764339	0.000761855	0.000764389	0.000360568	0.00318613
6	I_off (A/um)	4.16873E-07	4.78308E-07	4.84585E-07	4.84654E-07	1.7402E-12	7.84648E-06
7	C_tot	1	1.2076	1.081594	1.081594	1.081594	4.47
8							
9							
10	V_dd (V)	1.8	1.8	1.8	1.8	1.8	1.8
11	I_on (uA/um)	587.941	764.339	761.855	764.389	360.568	3186.13
12	I_off (nA/um)	416.873	478.308	484.585	484.654	0.0017402	7846.48
13	C_tot	1	1.2076	1.081594	1.081594	1.081594	4.47
14							
15							
16	Leakage Energy (pJ)	36.17	36.61	34.43	34.33	0.001482	452.3
17	Dynamic Energy (pJ)	10.26	11.6	10.79	10.79	10.79	32.79
18	Total Energy (pJ)	46.43	48.21	45.22	45.11	10.79	485.1
19	Clock Frequency(GHz)	0.1706	0.1934	0.2083	0.209	0.09988	0.2567
20	EDP (ns*pJ)	272.2	249.3	217.1	215.9	108	1890
21				Meets Spec	Better	WORSE	WORSE

Figure 6: Progressive Changes in Critical Outputs

After meeting spec, we noticed that we had seen noticeable improvements in all energy categories except Dynamic Energy. Our Dynamic Energy of the model running at $1.8V$ was $10.70pJ$ which was higher than our original. We decided that we could sacrifice some Clock Frequency, where we had some leeway, and further improve our Dynamic Energy expenditure. Noting that Vdd plays a key factor in our clock frequency, we decided to observe the impact that V_{dd} had on the EDP, given that we were operating with the transistor design that afforded us the most success. Initially, we were unsure of the impact

that changing V_{dd} would have on our results, especially since they both show up in various parts of the total energy equation. We decided to sift through a range of values, and see if we could determine a trend in the data, and hopefully come to a mathematical resolution that would explain what we were seeing. Over the range $0.4V - 1.8V$, we observed the impact that V_{dd} had on our EDP. As expected, as we decreased V_{dd}, our EDP decreased,

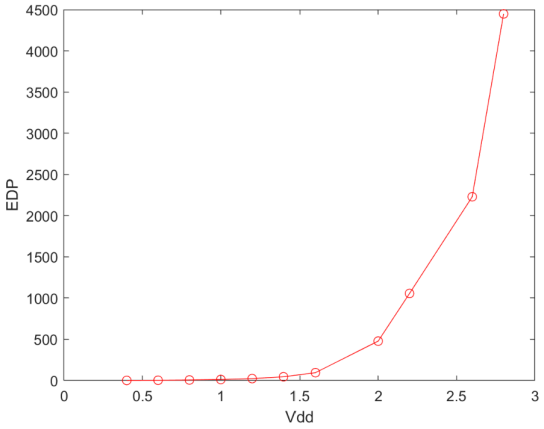

Figure 7: M3 Plot of Vdd vs EDP

which at first seemed like a major red flag. If that was truly the case, 0.4V would be optimal. However, upon second inspection, we noted that the change in V_{dd} showed itself in the Clock Frequency, which decreased after 1.7 V. After attempting values in the 1.8 V Range we decided the optimal value for our current design that met spec and improved our dynamic energy was 1.75V.

25				Optimal V_dd given M3				
26	V_dd (V)	I_on (uA/um)	I_off (nA/um)	Leakage Energy (pJ)	Dynamic Energy (pJ)	Total Energy (pJ)	Clock Frequency(GHz)	EDP(ns*pJ)
27	Standard (@1.8)	587.941	416.873	36.17	10.26	46.43	0.1706	272.2
28	1.8	764.389	484.654	34.33	10.79	45.11	0.209	215.9
29	1.75	740.727	402.766	27.82	10.2	38.02	0.2083	182.5 OPTIMAL
30	1.7	682.016	333.478	23.58	9.621	33.2	0.1977	168
31	1.6	618.483	226.028	15.6	8.522	24.12	0.1906	126.5
32	1.4	490.149	98.9902	6.585	6.525	13.11	0.173	75.77
33								

Figure 8: Optimal Vdd given Transistor Design M3

6 Calculations

The majority of our calculations were handled by MATLAB and Sentaurus, however, we did have to calculate Capacitance on our own. Rather than do it by hand, I wrote a brief MATLAB script to do these calculations for me.

$$C_{GC} = \frac{L_s \epsilon_{OX}}{t_s}$$

$$C_{GC} = \frac{L_{OX} \epsilon_{OX}}{t_{OX}}$$

Using these equations an adjusting them accordingly to changes in t_{oxide}, and ϵ, I could calculate the new gate capacitance, and take the ratio between the two quantities to determine the ratio required for the ARM MATLAB simulator.

```
%6.012 Design Project
%David Ologan 05/05/22

%Gate Capacitance Calculations

%Original MOSFET
L_s = 50*10^-7; % in cm
t_s = 35*10^-7; % in cm
L_ox = 35*10^-7; % in cm
t_ox = 5*10^-7; % in cm
e_ox_gc = 3.9*8.854*10^-14; %in F/cm
e_ox_gs = 3.9*8.854*10^-14; %in F/cm
C_gs = (L_s*e_ox_gs)/t_s
C_gc = (L_ox*e_ox_gc)/t_ox
C_gate = C_gs + C_gc % in F/cm

%Modified MOSFET
L_s_m = 50*10^-7; % in cm
t_s_m = 35*10^-7; % in cm
L_ox_m = 35*10^-7; % in cm
t_ox_m = 4*10^-7; % in cm
e_ox_gc_m = 3.9*8.854*10^-14; %in F/cm
e_ox_gs_m = 1*8.854*10^-14; %in F/cm
C_gs_m = (L_s_m*e_ox_gs_m)/t_s_m
C_gc_m = (L_ox_m*e_ox_gc_m)/t_ox_m
C_gate_m = C_gs_m + C_gc_m % in F/cm

%Ratio of Modified to Original
r = C_gate_m/C_gate
```

Figure 9: MATLAB Script to automate Capacitance Calculations

7 References

- Park Jae Beom. Atomic Layer Etching of Ultra-thin HfO2 film for gate oxide in MOSFET devices. Journal of Physics D: Applied Physics. https://iopscience.iop.org/article/10.1088/0022-3727/42/5/055202
- Leskela Markku. Rare Earth oxide thin films as gate oxides in MOSFET transistors. https://doi.org/10.1016/S0022-4596(02)00204-9